

# DATA SHEET

## **74LVC541A**

Octal buffer/line driver with 5 V  
tolerant inputs/outputs (3-state)

Product specification  
Supersedes data of 2003 May 14

2003 Nov 12

## Octal buffer/line driver with 5 V tolerant inputs/outputs (3-state)

## 74LVC541A

### FEATURES

- 5 V tolerant inputs/outputs; for interfacing with 5 V logic
- Wide supply voltage range from 2.7 to 3.6 V
- CMOS low-power consumption
- Direct interface with TTL levels
- Complies with JEDEC standard no. 8-1A
- ESD protection:  
HBM EIA/JESD22-A114-A exceeds 2000 V  
MM EIA/JESD22-A115-A exceeds 200 V.

### DESCRIPTION

The 74LVC541A is a high performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

This device is fully specified for partial power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

Inputs can be driven from either 3.3 or 5 V devices. In 3-state operation, outputs can handle 5 V. This feature allows the use of these devices as translators in a mixed 3.3 and 5 V environment.

The 74LVC541A is an octal non-inverting buffer/line driver with 5 V tolerant inputs/outputs. The 3-state outputs are controlled by the output enable inputs OE1 and OE2.

### QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $t_r = t_f \leq 2.5\text{ ns}$ .

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	propagation delay An to Yn	$C_L = 50\text{ pF}$ ; $V_{CC} = 3.3\text{ V}$	3.3	ns
$C_I$	input capacitance		5.0	pF
$C_{PD}$	power dissipation capacitance per buffer	$V_{CC} = 3.3\text{ V}$ ; notes 1 and 2	20	pF

### Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  
 $f_o$  = output frequency in MHz;  
 $C_L$  = output load capacitance in pF;  
 $V_{CC}$  = supply voltage in Volts;  
 $N$  = total load switching outputs;  
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.
2. The condition is  $V_I = \text{GND to } V_{CC}$ .

# Octal buffer/line driver with 5 V tolerant inputs/outputs (3-state)

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**FUNCTION TABLE**

See note 1.

INPUT			OUTPUT
$\overline{OE}1$	$\overline{OE}2$	$A_n$	$Y_n$
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

**Note**

- H = HIGH voltage level;  
L = LOW voltage level;  
X = don't care;  
Z = high-impedance OFF-state.

**ORDERING INFORMATION**

TYPE NUMBER	TEMPERATURE RANGE	PACKAGE			
		PINS	PACKAGE	MATERIAL	CODE
74LVC541AD	-40 to +125 °C	20	SO20	plastic	SOT163-1
74LVC541ADB	-40 to +125 °C	20	SSOP20	plastic	SOT339-1
74LVC541APW	-40 to +125 °C	20	TSSOP20	plastic	SOT360-1
74LVC541ABQ	-40 to +125 °C	20	DHVQFN20	plastic	SOT764-1

**PINNING**

PIN	SYMBOL	DESCRIPTION
1	$\overline{OE}1$	output enable input (active LOW)
2	A0	data input
3	A1	data input
4	A2	data input
5	A3	data input
6	A4	data input
7	A5	data input
8	A6	data input
9	A7	data input
10	GND	ground (0 V)

PIN	SYMBOL	DESCRIPTION
11	Y7	bus output
12	Y6	bus output
13	Y5	bus output
14	Y4	bus output
15	Y3	bus output
16	Y2	bus output
17	Y1	bus output
18	Y0	bus output
19	$\overline{OE}2$	output enable input (active LOW)
20	$V_{CC}$	supply voltage

Octal buffer/line driver with 5 V tolerant inputs/outputs (3-state)

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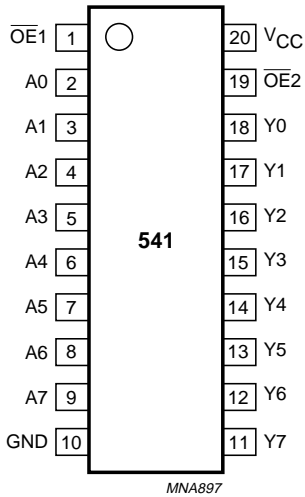
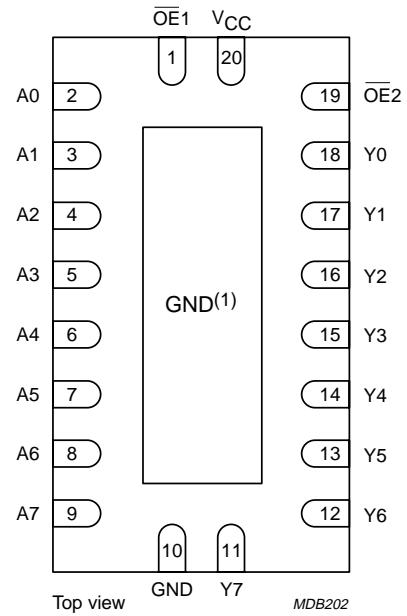


Fig.1 Pin configuration SO20 and (T)SSOP20.



(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.2 Pin configuration DHVQFN20.

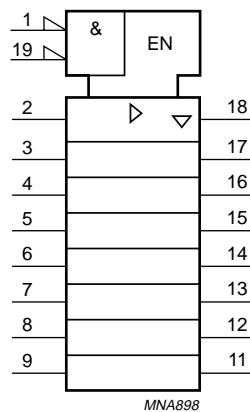


Fig.3 Logic Symbol (IEEE/IEC).

# Octal buffer/line driver with 5 V tolerant inputs/outputs (3-state)

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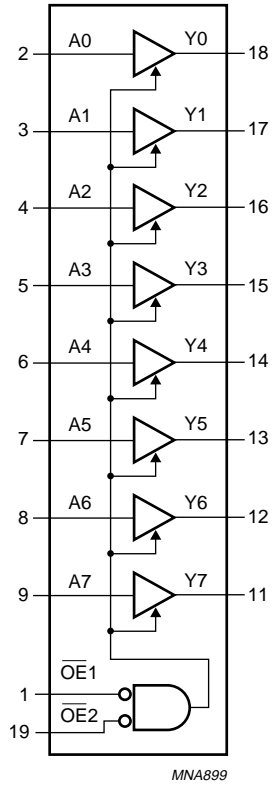


Fig.4 Logic symbol.

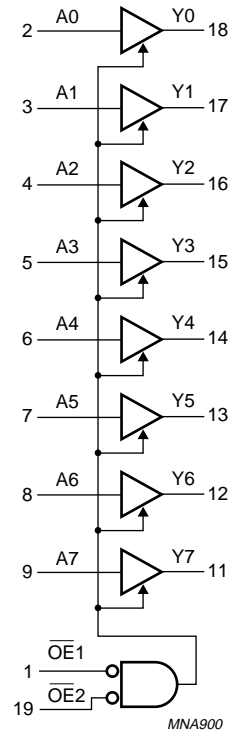


Fig.5 Functional diagram.

# Octal buffer/line driver with 5 V tolerant inputs/outputs (3-state)

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC</sub>	supply voltage	for maximum speed performance	2.7	3.6	V
		for low-voltage applications	1.2	3.6	V
V <sub>I</sub>	input voltage		0	5.5	V
V <sub>O</sub>	output voltage	output HIGH or LOW state	0	V <sub>CC</sub>	V
		output 3-state	0	5.5	V
T <sub>amb</sub>	operating ambient temperature	in free air	-40	+125	°C
t <sub>r</sub> , t <sub>f</sub>	input rise and fall times	V <sub>CC</sub> = 1.2 to 2.7 V	0	20	ns/V
		V <sub>CC</sub> = 2.7 to 3.6 V	0	10	ns/V

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC</sub>	supply voltage		-0.5	+6.5	V
I <sub>IK</sub>	input diode current	V <sub>I</sub> < 0	-	-50	mA
V <sub>I</sub>	input voltage	note 1	-0.5	+5.5	V
I <sub>OK</sub>	output diode current	V <sub>O</sub> > V <sub>CC</sub> or V <sub>O</sub> < 0	-	±50	mA
V <sub>O</sub>	output voltage	output HIGH or LOW state; note 1	-0.5	V <sub>CC</sub> + 0.5	V
		output 3-state or power down; note 1	-0.5	+6.5	V
I <sub>O</sub>	output diode source or sink current	V <sub>O</sub> = 0 to V <sub>CC</sub>	-	±50	mA
I <sub>CC</sub> , I <sub>GND</sub>	V <sub>CC</sub> or GND current		-	±100	mA
T <sub>stg</sub>	storage temperature		-60	+150	°C
P <sub>tot</sub>	power dissipation	T <sub>amb</sub> = -40 to +125 °C; note 2	-	500	mW

## Notes

- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- For SO20 packages: above 70 °C the value of P<sub>tot</sub> derates linearly with 8 mW/K.  
For (T)SSOP20 packages: above 60 °C the value of P<sub>tot</sub> derates linearly with 5.5 mW/K.  
For DHVQFN20 packages: above 60 °C the value of P<sub>tot</sub> derates linearly with 4.5 mW/K.

# Octal buffer/line driver with 5 V tolerant inputs/outputs (3-state)

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## DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. <sup>(1)</sup>	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.2	V <sub>CC</sub>	–	–	V
			2.7 to 3.6	2.0	–	–	V
V <sub>IL</sub>	LOW-level input voltage		1.2	–	–	0	V
			2.7 to 3.6	–	–	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -100 µA	2.7 to 3.6	V <sub>CC</sub> - 0.2	V <sub>CC</sub>	–	V
		I <sub>O</sub> = -12 mA	2.7	V <sub>CC</sub> - 0.5	–	–	V
		I <sub>O</sub> = -18 mA	3.0	V <sub>CC</sub> - 0.6	–	–	V
		I <sub>O</sub> = -24 mA	3.0	V <sub>CC</sub> - 0.8	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 100 µA	2.7 to 3.6	–	0	0.2	V
		I <sub>O</sub> = 12 mA	2.7	–	–	0.4	V
		I <sub>O</sub> = 24 mA	3.0	–	–	0.55	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND	3.6	–	±0.1	±5	µA
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5 V or GND	3.6	–	±0.1	±5	µA
I <sub>off</sub>	power-off leakage supply	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0.0	–	±0.1	±10	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	3.6	–	0.1	10	µA
ΔI <sub>CC</sub>	additional quiescent supply current per pin	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0	2.7 to 3.6	–	5	500	µA

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. <sup>(1)</sup>	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.2	V <sub>CC</sub>	–	–	V
			2.7 to 3.6	2.0	–	–	V
V <sub>IL</sub>	LOW-level input voltage		1.2	–	–	0	V
			2.7 to 3.6	–	–	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -100 µA	2.7 to 3.6	V <sub>CC</sub> - 0.3	–	–	V
		I <sub>O</sub> = -12 mA	2.7	V <sub>CC</sub> - 0.65	–	–	V
		I <sub>O</sub> = -18 mA	3.0	V <sub>CC</sub> - 0.75	–	–	V
		I <sub>O</sub> = -24 mA	3.0	V <sub>CC</sub> - 1	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 100 µA	2.7 to 3.6	–	–	0.3	V
		I <sub>O</sub> = 12 mA	2.7	–	–	0.6	V
		I <sub>O</sub> = 24 mA	3.0	–	–	0.8	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND	3.6	–	–	±20	µA
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5 V or GND	3.6	–	–	±20	µA
I <sub>off</sub>	power-off leakage supply	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0.0	–	–	±20	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	3.6	–	–	40	µA
ΔI <sub>CC</sub>	additional quiescent supply current per pin	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0	2.7 to 3.6	–	–	5000	µA

**Note**1. All typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.



# Octal buffer/line driver with 5 V tolerant inputs/outputs (3-state)

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**AC CHARACTERISTICS**GND = 0 V;  $t_r = t_f \leq 2.5$  ns;  $C_L = 50$  pF.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. <sup>(1)</sup>	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay An to Yn	see Figs 6 and 8	1.2	–	14	–	ns
			2.7	1.5	3.9	5.6	ns
			3.0 to 3.6	1.0	3.3 <sup>(2)</sup>	5.1	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time OEn to Yn	see Figs 7 and 8	1.2	–	20	–	ns
			2.7	1.5	5.2	7.5	ns
			3.0 to 3.6	1.0	4.4 <sup>(2)</sup>	7.0	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time OEn to Yn	see Figs 7 and 8	1.2	–	11	–	ns
			2.7	1.5	4.3	7.0	ns
			3.0 to 3.6	1.0	3.8 <sup>(2)</sup>	6.0	ns
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay An to Yn	see Figs 6 and 8	1.2	–	–	–	ns
			2.7	1.5	–	7.0	ns
			3.0 to 3.6	1.0	–	6.5	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time OEn to Yn	see Figs 7 and 8	1.2	–	–	–	ns
			2.7	1.5	–	9.5	ns
			3.0 to 3.6	1.0	–	9.0	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time OEn to Yn	see Figs 7 and 8	1.2	–	–	–	ns
			2.7	1.5	–	9.0	ns
			3.0 to 3.6	1.0	–	7.5	ns

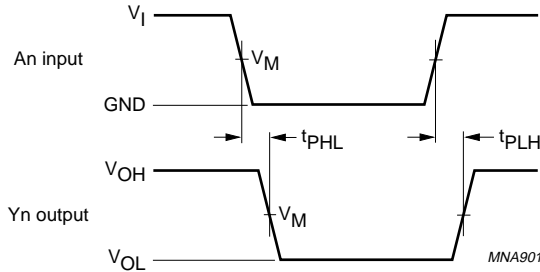
**Notes**

1. All typical values are measured T<sub>amb</sub> = 25 °C.
2. These typical values are measured at V<sub>CC</sub> = 3.3 V.

Octal buffer/line driver with 5 V tolerant inputs/outputs (3-state)

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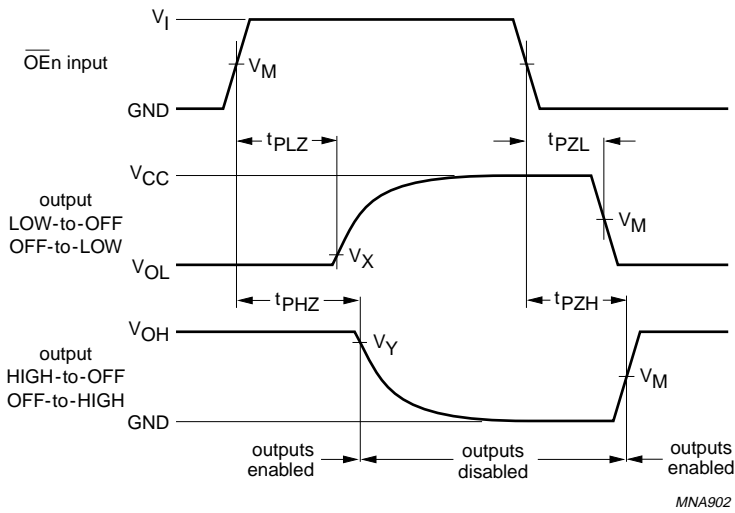
AC WAVEFORMS



V <sub>CC</sub>	V <sub>M</sub>	INPUT	
		V <sub>I</sub>	t <sub>r</sub> = t <sub>f</sub>
1.2 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>	≤ 2.5 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns

V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage drop that occur with the output load.

Fig.6 Input (An) to output (YN) propagation delays.



V <sub>CC</sub>	V <sub>M</sub>	INPUT	
		V <sub>I</sub>	t <sub>r</sub> = t <sub>f</sub>
1.2 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>	≤ 2.5 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns

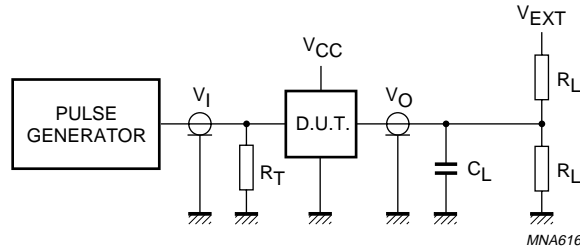
V<sub>X</sub> = V<sub>OL</sub> + 0.3 V at V<sub>CC</sub> ≥ 2.7 V;  
 V<sub>X</sub> = V<sub>OL</sub> + 0.1 V at V<sub>CC</sub> < 2.7 V;  
 V<sub>Y</sub> = V<sub>OH</sub> - 0.3 V at V<sub>CC</sub> ≥ 2.7 V;  
 V<sub>Y</sub> = V<sub>OH</sub> - 0.1 V at V<sub>CC</sub> < 2.7 V.

V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage drop that occur with the output load.

Fig.7 3-state enable and disable times.

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V <sub>CC</sub>	V <sub>I</sub>	C <sub>L</sub>	R <sub>L</sub>	V <sub>EXT</sub>		
				t <sub>PLH</sub> /t <sub>PHL</sub>	t <sub>PZH</sub> /t <sub>PHZ</sub>	t <sub>PZL</sub> /t <sub>PLZ</sub>
1.2 V	V <sub>CC</sub>	50 pF	500 Ω <sup>(1)</sup>	open	GND	2 × V <sub>CC</sub>
2.7 V	2.7 V	50 pF	500 Ω	open	GND	2 × V <sub>CC</sub>
3.0 to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	2 × V <sub>CC</sub>

**Note**

1. The circuit performs better when R<sub>L</sub> = 1000 Ω.

Definitions for test circuits:

R<sub>L</sub> = Load resistor.

C<sub>L</sub> = Load capacitance including jig and probe capacitance.

R<sub>T</sub> = Termination resistance should be equal to the output impedance Z<sub>o</sub> of the pulse generator.

Fig.8 Load circuitry for switching times.

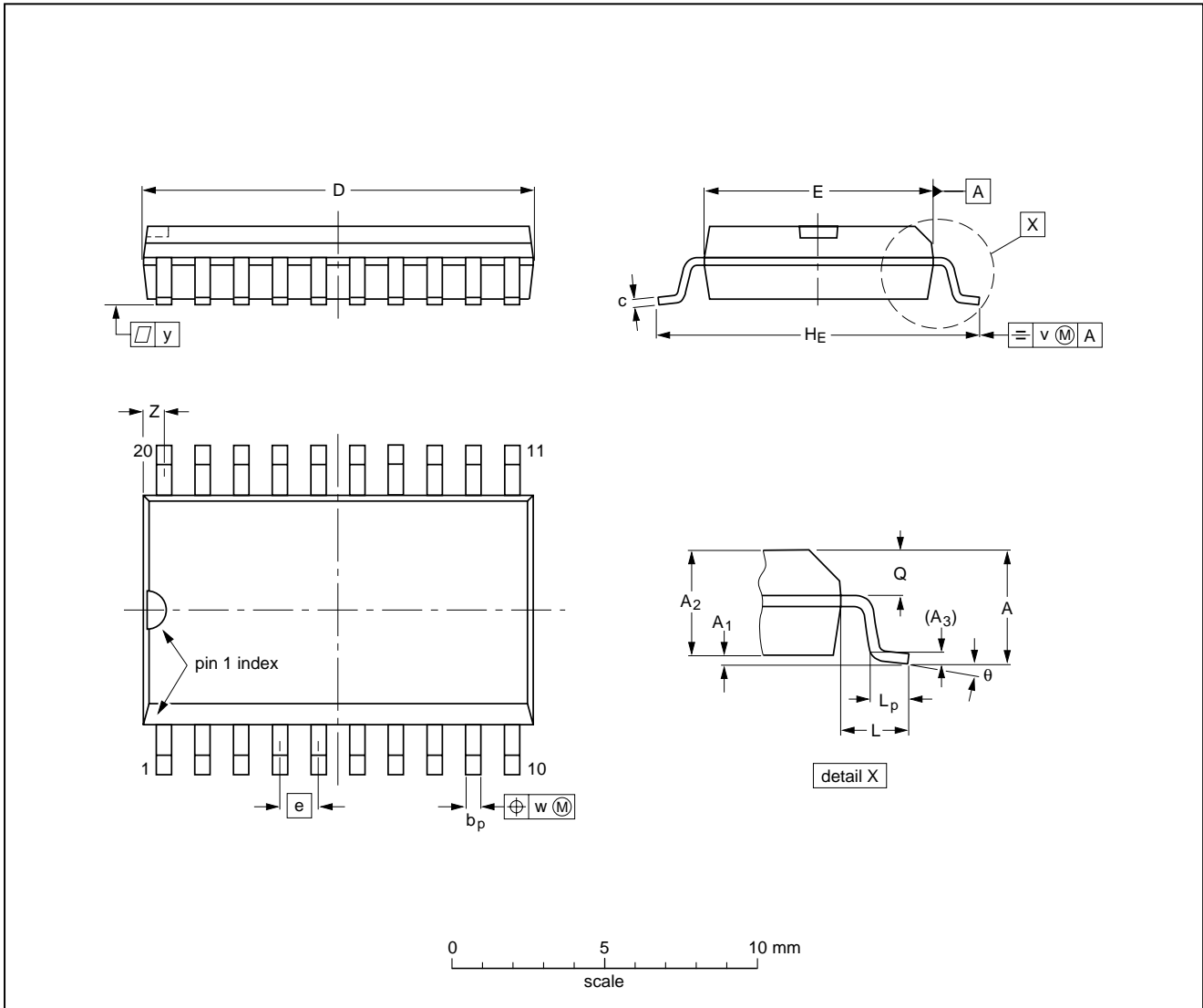
Octal buffer/line driver with 5 V tolerant inputs/outputs (3-state)

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PACKAGE OUTLINES

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

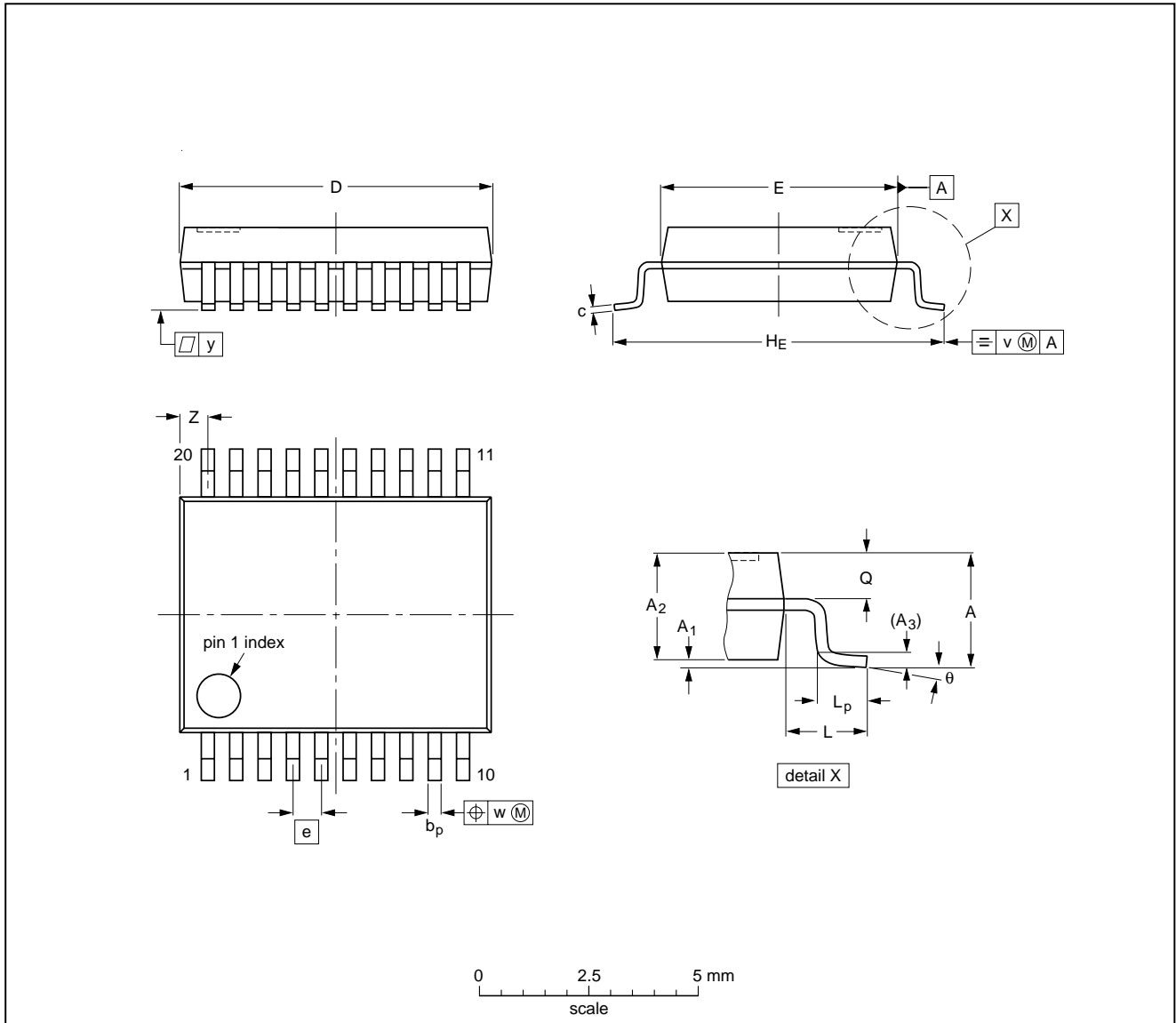
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT163-1	075E04	MS-013			99-12-27 03-02-19

Octal buffer/line driver with 5 V tolerant inputs/outputs (3-state)

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SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

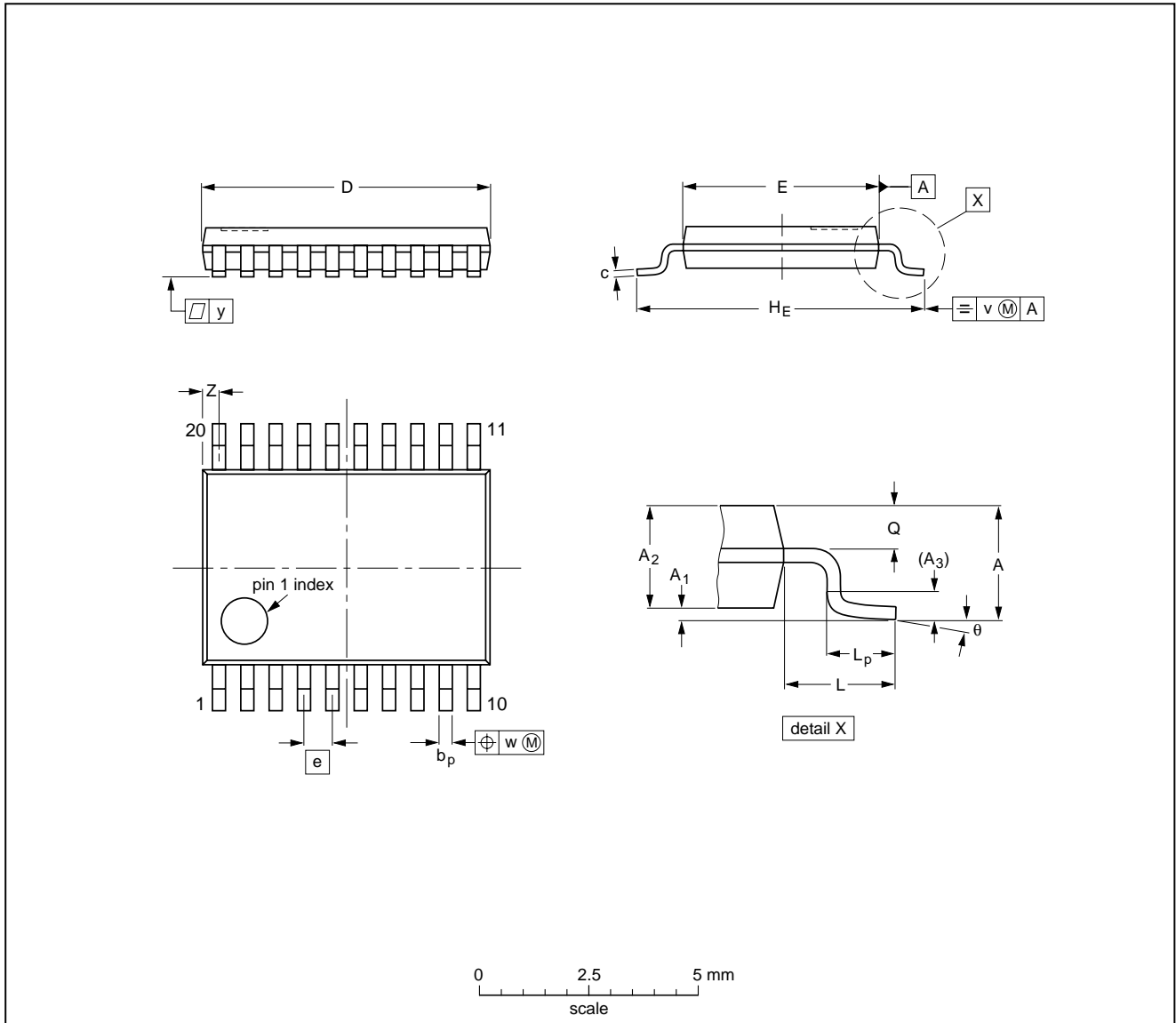
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT339-1		MO-150				99-12-27 03-02-19

Octal buffer/line driver with 5 V tolerant inputs/outputs (3-state)

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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

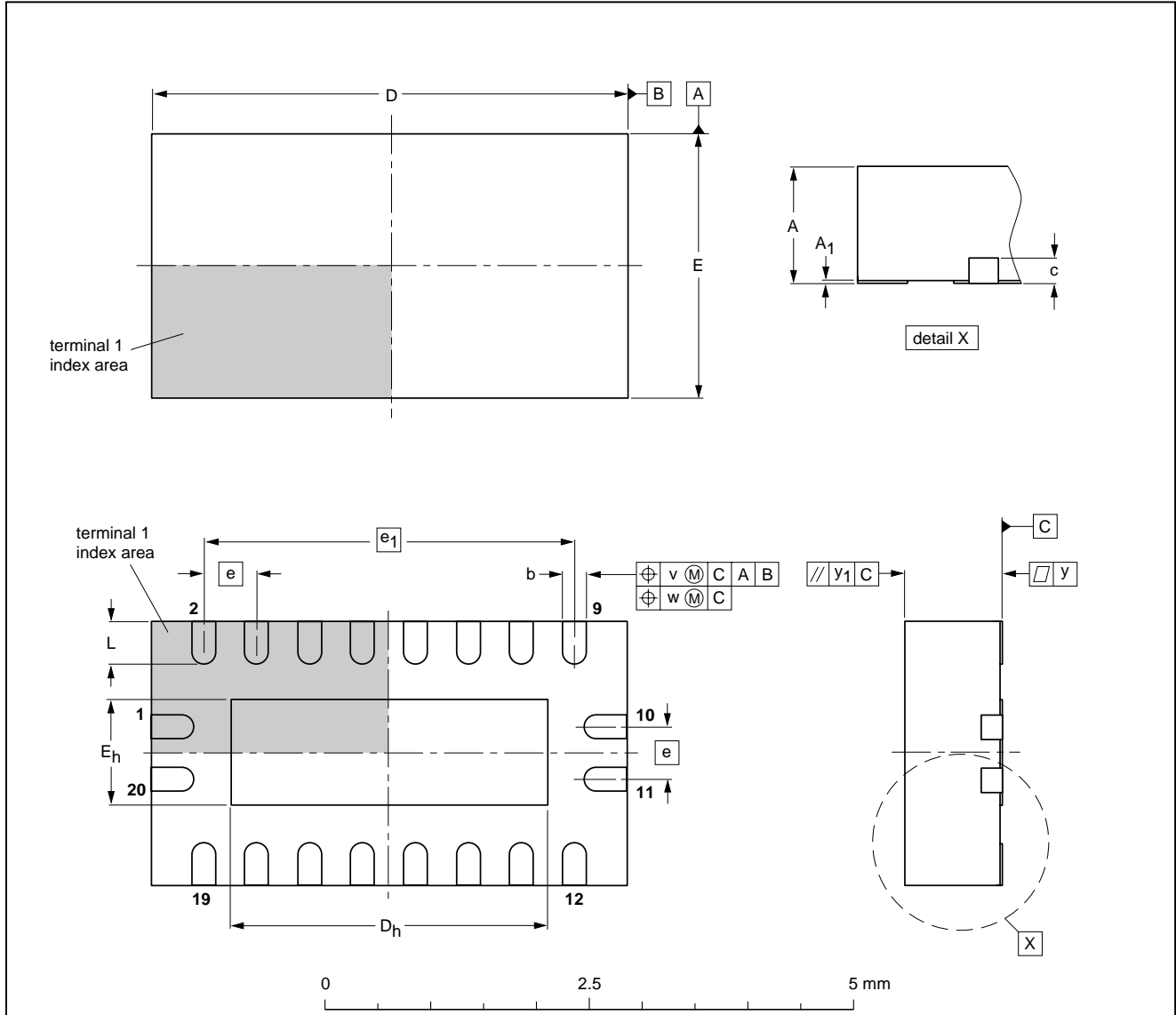
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				99-12-27 03-02-19

# Octal buffer/line driver with 5 V tolerant inputs/outputs (3-state)

74LVC541A

**DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm**

**SOT764-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A <sup>(1)</sup> max.	A <sub>1</sub>	b	c	D <sup>(1)</sup>	D <sub>h</sub>	E <sup>(1)</sup>	E <sub>h</sub>	e	e <sub>1</sub>	L	v	w	y	y <sub>1</sub>
mm	1	0.05 0.00	0.30 0.18	0.2	4.6 4.4	3.15 2.85	2.6 2.4	1.15 0.85	0.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

**Note**  
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT764-1	---	MO-241	---		02-10-17 03-01-27

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## DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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## **Contact information**

For additional information please visit <http://www.semiconductors.philips.com>. Fax: +31 40 27 24825

For sales offices addresses send e-mail to: [sales.addresses@www.semiconductors.philips.com](mailto:sales.addresses@www.semiconductors.philips.com).

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